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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,892	11/21/2003	David W. Nippa	OPI 0004 PA/41004.11	1439

23368 7590 06/27/2007

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EXAMINER	
RAHLL, JERRY T	

ART UNIT	PAPER NUMBER
2874	

MAIL DATE	DELIVERY MODE
06/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/719,892	NIPPA ET AL.	
	Examiner	Art Unit	
	Jerry T. Rahll	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *61-117,119 and 120* is/are pending in the application.

4a) Of the above claim(s) *68-73* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-67,74-117,119 and 120* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 16, 2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 63-66, 105, 106, 108, 117, and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,711,308 to Erben et al.

5. Regarding Claim 63, Erben et al. describes a method of fabricating an integrated optical device including providing a support wafer (32), forming an electrode pattern (44) on the support wafer to define two electrically isolated control electrodes, forming a non-polymeric buffer layer (38'', Column 6 Lines 30-33) on the electrode pattern and support wafer, forming a waveguide core material (48) over the buffer layer with a pair of cladding containment regions (from left side to 50 and from right side to 52, see Figure 7) along the sides of the core in a direction parallel to the longitudinal dimension of the core, where each of the cladding containment regions are defined between pairs of opposing sidewalls (sidewalls of the waveguides 50 and 52 and modulator sidewalls shown in Figure 7), and positioning a cladding material (36'') within the cladding containment regions in optical communication with the core to define an optically clad waveguide core, where an electrically insulative barrier (38'') layer is formed over the control electrodes prior to positioning the cladding, and where a control signal applied to the electrodes alters a transmission characteristic (see Column 5 Lines 23-47) of an optical signal traveling along the waveguide core (see Figure 7 and Columns 4-6 and 9). Erben et al. does not specifically describe removing portions of the core material layer to define the waveguide core (50, 52). Erben et al. is silent on the method of forming the waveguide core structure. However, removal of core material from a layer is a well-known method of forming cores, such as that described by Erben et al. Therefore, it would have been obvious to one of ordinary skill in the art to remove some of the core material to form the cores described by Erben et al. The motivation for doing so would have been to create the desired shape of the waveguides using known methods such as milling or etching.

6. Regarding Claim 64, Erben et al. describes the insulative barrier formed on the electrodes as a layer of silica (see Column 6 Lines 30-33).

7. Regarding Claim 65, Erben et al. describes the buffer layer formed over the electrodes to form the electrically insulative barrier (see Figure 2).

8. Regarding Claim 66, Erben et al. describes the electrodes (44) formed co-planar (see Figure 2).

9. Regarding Claim 105, Erben et al. describes a method of fabricating an integrated optical device including providing a support wafer (32), forming an electrode pattern (44) on the support wafer, forming a non-polymeric buffer layer (38'', Column 6 Lines 30-33) on the electrode pattern and support wafer, forming a waveguide core material (48) over the buffer layer with a pair of cladding containment regions (from left side to 50 and from right side to 52, see Figure 7) along the sides of the core in a direction parallel to the longitudinal dimension of the core, where each of the cladding containment regions are defined between pairs of opposing sidewalls (sidewalls of the waveguides 50 and 52 and modulator sidewalls shown in Figure 7), and positioning a cladding material (36'') within the cladding containment regions and in optical communication with the core to define an optically clad waveguide core while a poling voltage is applied across the electrode pattern (the Examiner notes that the poling voltage may be zero), where a control signal applied to the electrodes alters a transmission characteristic (see Column 5 Lines 23-47) of an optical signal traveling along the waveguide core (see Figure 7 and Columns 4-6 and 9).. Erben et al. does not specifically describe removing portions of the ore material layer to define the waveguide core (50, 52). Erben et al. is silent on the method of forming the waveguide core structure. However, removal of core material form a layer is a well-known

method of forming cores, such as that described by Erben et al. Therefore, it would have been obvious to one of ordinary skill in the art to remove some of the core material to form the cores described by Erben et al. The motivation for doing so would have been to create the desired shape of the waveguides using known methods such as milling or etching.

10. Regarding Claim 106, while Erben et al. does not specifically point out that the voltage is maintained during the curing, cross-linking, or thermo-setting of the cladding material, a the polymer nature of the cladding material would inherently have such a curing, cross-linking, or thermo-setting step involved in it s production.

11. Regarding Claim 108, Erben et al. describes the formation of an electrically insulative barrier layer (38'') formed over the electrode pattern.

12. Regarding Claim 117, Erben et al. describes a method of fabricating an integrated optical device including providing a support wafer (32), forming an electrode pattern (44) on the support wafer, forming a non-polymeric buffer layer (38'', Column 6 Lines 30-33) on the electrode pattern and support wafer, forming a waveguide core material (48) over the buffer layer with a pair of cladding containment regions (from left side to 50 and from right side to 52, see Figure 7) along the sides of the core in a direction parallel to the longitudinal dimension of the core, where each of the cladding containment regions are defined between pairs of opposing sidewalls (sidewalls of the waveguides 50 and 52 and modulator sidewalls shown in Figure 7), and positioning a cladding material (36'') within the cladding containment regions and in optical communication with the core to define an optically clad waveguide core while a poling voltage is applied across the electrode pattern (the Examiner notes that the poling voltage may be zero), where a control signal applied to the electrodes alters a transmission characteristic (see Column 5

Lines 23-47) of an optical signal traveling along the waveguide core (see Figure 7 and Columns 4-6 and 9). Erben et al. does not specifically describe removing portions of the ore material layer to define the waveguide core (50, 52). Erben et al. is silent on the method of forming the waveguide core structure. However, removal of core material form a layer is a well-known method of forming cores, such as that described by Erben et al. Therefore, it would have been obvious to one of ordinary skill in the art to remove some of the core material to form the cores described by Erben et al. The motivation for doing so would have been to create the desired shape of the waveguides using known methods such as milling or etching.

13. Regarding Claim 119, Erben et al. describes a method of fabricating an integrated optical device including providing a support wafer (32), forming an electrode pattern (44) on the support wafer, forming a buffer layer (38'', Column 6 Lines 30-33) on the electrode pattern and support wafer, forming a waveguide core (48) over the buffer layer with a pair of cladding containment regions (from left side to 50 and from right side to 52, see Figure 7) along the sides of the core in a direction parallel to the longitudinal dimension of the core, where each of the cladding containment regions are defined between pairs of opposing sidewalls (sidewalls of the waveguides 50 and 52 and modulator sidewalls shown in Figure 7),and positioning a cladding material (36'') between the cladding containment regions and in optical communication with the core to define an optically clad waveguide core while a poling voltage is applied across the electrode pattern (the Examiner notes that the poling voltage may be zero), where a control signal applied to the electrodes alters a transmission characteristic (see Column 5 Lines 23-47) of an optical signal traveling along the waveguide core (see Figure 7 and Columns 4-6 and 9). Erben et al. does not specifically describe the formation of the buffer layer via a sol-gel process.

However, sol-gel processes are all well-known methods of forming a silica substrate, as described by Erben et al. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use a sol-gel process to form the buffer layer of Erben et al. The motivation for doing so would have been to produce the described device in an accurate and efficient manner.

14. Claims 61, 62, 67, 74-96, 100-104, 109-116, and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erben et al. in view of US Patent No. 5,857,039 to Bosc.

15. Regarding Claim 61, Erben et al. describes a method of fabricating an integrated optical device including providing a support wafer (32), forming an electrode pattern (44) on the support wafer, forming a non-polymeric buffer layer (38'', Column 6 Lines 30-33) on the electrode pattern and support wafer, forming a waveguide core material (48) over the buffer layer with a pair of cladding containment regions (from left side to 50 and from right side to 52, see Figure 7) along the sides of the core in a direction parallel to the longitudinal dimension of the core, where each of the cladding containment regions are defined between pairs of opposing sidewalls (sidewalls of the waveguides 50 and 52 and modulator sidewalls shown in Figure 7), and positioning a cladding material (36'') within the cladding containment regions in optical communication with the core to define an optically clad waveguide core, where a control signal applied to the electrodes alters a transmission characteristic (see Column 5 Lines 23-47) of an optical signal traveling along the waveguide core (see Figure 7 and Columns 4-6 and 9). Erben et al. does not specifically describe the core material as a non-polymeric, silica-based waveguide core material or removing portions of the core material layer to define the waveguide core (50,

52). Bosc et al. describes a method of making an integrated optical device including providing a support wafer (22), forming an electrode pattern (32), forming a non-polymeric buffer layer (24) on the electrode pattern and support wafer, forming a non-polymeric, silica-based waveguide core material layer (25) over the buffer layer, removing portions of the core material layer (see Column 7, Lines 47-54) to define a non-polymeric waveguide core (26, 28), and positioning a cladding material (30) in optical communication with the core to define an optically clad waveguide core, where a control signal applied to the electrodes alters a transmission characteristic (see Column 6 Lines 6-16) of an optical signal traveling along the waveguide core. At the time of the invention it would have been obvious to one of ordinary skill in the art to use the core formation materials and method of Bosc et al. in the method of Erben et al. The motivation for doing so would have been to make the device compatible with an optical fiber transmitting optical energy (see Bosc et al. at Column 4 Lines 64-66).

16. The device of Claim 120 is an embodiment of the above-discussed method of Claim 61.

17. Regarding Claim 62, Erben et al. describes the electrode pattern, buffer layer and core formed such that the electrode pattern is embedded in the device beneath the waveguide core (see Figure 2).

18. Regarding Claim 67, Erben et al. describes the electrode pattern defining two isolated control electrodes (44) and the core positioned in a plane offset and parallel to the plane of the control electrodes (see Figure 2).

19. Regarding Claims 74 and 76, Erben et al. describes the electrode pattern including gold (see Column 5 Lines 23-24), which has a melting point greater than 1500°C).

20. Regarding Claim 75, Bosc et al. describe the electrodes as including chromium (see Column 7 Line 67). At the time of invention, it would have been obvious to one of ordinary skill in the art to use such well-known materials in the electrodes of Erben et al. The motivation for doing so would have been to utilize the structural properties of chromium.

21. Regarding Claim 77, neither Erben et al. nor Bosc et al. specifically describe the electrode pattern including a first conductive layer with increased adhesive properties and a second conductive layer with increased conductive properties. However, such electrode structures are well-known in the art. Therefore, at the time of invention it would have been obvious to one of ordinary skill in the art to use such a two-layer electrode structure. The motivation for doing so would have been to maximize structural and conductive properties of the electrode.

22. Regarding Claim 78, Erben et al. describes the buffer layer (38'') formed on both the electrode patter and support wafer (see Figure 2).

23. Regarding Claims 79-84, Erben et al. does not specifically describe the formation of the buffer layer via the methods outlined on the present claims. However, these methods are all well-known methods of forming a silica substrate, as described by Erben et al. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use any well-known method to form the silica substrate of Erben et al. The motivation for doing so would have been to produce the described device in an accurate and efficient manner.

24. Regarding Claim 85, Erben et al. describes the buffer layer ad silica-based (see Column 6 Lines 30-33).

25. Regarding Claim 86, Erben et al. does not specifically describe the step of removing portions of the buffer layer. However, it is well-known in the art to remove material from silica substrates via polishing. At the time of the invention, it would have been obvious to one of ordinary skill in the art to remove material form the buffer layer of Erben et al. via polishing. The motivation for doing so would have been to prepare the upper surface for forming additional layers on that surface.

26. Regarding Claim 87, Erben et al. describes the buffer layer (38'') formed of silica (see Column 6, Line 32). Further, Bosc et al. descries the core having a refractive index higher than silica (see Column 4 Lines 18-19). Therefore, the buffer layer of Erben et al. has a refractive index lower than the refractive index of the core material of the combined device.

27. Regarding Claim 88, Erben et al. describes the buffer layer material having a refractive index of about 1.450 (see Column 6 Line 35).

28. Regarding Claim 89, Erben et al. describes the buffer layer (38'') formed of silica (see Column 6, Line 32). Silica is transmissive of light at 1.3μm and 1.5μm.

29. Regarding Claim 90, Erben et al. describes the buffer layer (38'') formed of silica (see Column 6, Line 32). Silica is an electrically insulating, non-metallic material.

30. Regarding Claim 91, Bosc et al. describes the core layer material made from silica or doped silica (see Column 4 Lines 63-64).

31. Regarding Claims 92, Bosc et al. does not specifically describe the formation of the core layer via sol-gel process. Sol-gel processes are well-known methods of forming a silica structures. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to a sol-gel process to form the silica waveguide layer of Bosc et al. The

motivation for doing so would have been to produce the described device in an accurate and efficient manner.

32. Regarding Claim 93, Bosc et al. describes the core layer material having a refractive index of 1.4510 (Column 6 Line 52) and 1.4520 (Column 4 Line 18).

33. Regarding Claim 94, Bosc et al. describes the portions of core layer removed via reactive ion etching (see Column 7 Line 53).

34. Regarding Claim 95, Bosc et al. describes the waveguide core formed by patterning the core material layer utilizing a waveguide mask (see Column 7 Lines 47-53).

35. Regarding Claim 96, Erben et al. describes the cladding material comprising an electro optic medium (see Column 5 Line 19-Column 6 Line 49).

36. Regarding Claims 100-104, Erben et al. does not specifically describe the formation of the cladding via the methods outlined on the present claims. However, these methods are all well-known methods of forming a polymer structure, as described by Erben et al. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use any well-known method to form the polymer cladding of Erben et al. The motivation for doing so would have been to produce the described device in an accurate and efficient manner.

37. Regarding Claim 109, Erben et al. describes the cladding material having a thickness at least as large as the thickness defined by the core material layer (see Figure 2).

38. Regarding Claim 110, Erben et al. describes further portions of the core material layer and buffer layer removed to define a pair of contact regions on the electrode pattern (See Figure 7).

39. Regarding Claim 111, Erben et al. does not specifically describe the contact regions treated with hydrofluoric acid to remove residual material. However, such use of hydrofluoric acid is well-known in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use hydrofluoric acid on the device of Erben et al. The motivation for doing so would have been to ensure proper electrical connection at the contact regions.

40. Regarding Claims 112 and 113, Erben et al. does not specifically describe the step of removing portions of the buffer layer. However, it is well-known in the art to remove material from silica substrates via polishing. At the time of the invention, it would have been obvious to one of ordinary skill in the art to remove material form the buffer layer of Erben et al. via polishing. The motivation for doing so would have been to prepare the upper surface for forming additional layers on that surface. The upper surface of the buffer layer defines a core material containment region (see Figure 2).

41. Regarding Claims 114 and 116, Bosc et al. describes the waveguide core material formed within the core material confinement region defined by the buffer layer (region along entire width of buffer layer; see Figures 3, 4A-4C, and 6D).

42. Regarding Claim 115, Bosc et al. describes the waveguide core material extending beyond the core material confinement region defined by the buffer layer (region only at core sections with material outside the core sections see Figures 6C-6D).

43. Claims 97 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erben et al. as applied to Claims 66 and 105 above, and further in view of US Patent No. 5,093,883 to Yoon et al.

44. Regarding Claims 97 and 107, Erben does not specifically describe the cladding material comprising an electro-optic chromophore. Yoon et al. describes electro-optic chromophore materials (see Column 6 Lines 40''-45). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the chromophore material of Yoon et al. in the cladding of Erben et al. The motivation for doing so would have been to allow more precise control of optical characteristics via electrical control signals.

45. Claim 98 is rejected under 35 U.S.C. 103(a) as being unpatentable over Erben et al. as applied to Claims 96 above, and further in view of US Patent No. 5,093,883 to Yoon et al.

46. Erben does not specifically describe the cladding material dominated by the Pockels effect. Yoon et al. describes electro-optic material dominated by the Pockels effect (see Column 5 Line 58). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the material of Yoon et al. in the cladding of Erben et al. The motivation for doing so would have been to allow more precise control of optical characteristics via electrical control signals.

47. Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Erben et al. as applied to Claims 96 above, and further in view of US Patent No. 6,693,736'' to Yoshimura et al.

48. Erben does not specifically describe the cladding material dominated by the Kerr effect. Yoshimura et al. describes electro-optic material dominated by the Kerr effect (see Column 34 Lines 53-56). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the material of Yoshimura et al. in the cladding of Erben et al. The motivation for doing so would have been to allow more precise control of optical characteristics via electrical control signals.

Response to Arguments

49. Applicant's arguments, with respect to 118 have been fully considered and are persuasive. The Examiner overlooked the cancellation of Claim 118 in Applicant's amendment received September 14, 2006. The rejection of Claim 118 has been withdrawn.

50. Applicant's arguments regarding independent Claims 61, 63, 105, 117, 119-120 are not persuasive in view of the current rejection under Eerben et al. The Examiner directs Applicant to Figure 7 of Erben et al., showing cladding containment regions defined between pairs of sidewalls. The defining sidewalls are the outer sidewalls of the cores 50 and 52 and the modulator sidewalls shown in the Figure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerry T. Rahll whose telephone number is (571) 272-2356. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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6/25/07